

CLAIM AMENDMENTS

IN THE CLAIMS

This listing of the claims will replace all prior versions, and listing, of claims in the application or previous response to office action:

1. **(Currently Amended)** An integrated circuit comprising function modules, wherein the function modules comprise:

a central processing unit designed to process data and to execute programs, **and**

a cache memory, ~~wherein the function modules comprise~~

an encryption unit designed to encrypt and decrypt data, ~~and the function modules comprise~~

a security sensor system including a protective layer on the integrated circuit including at least one elongated electrical line extending along the surface of the integrated circuit, the security sensor system operable to:

monitor ~~the state~~ an ohmic resistance of at least one electrical line of the protective layer on the integrated circuit,

compare the monitored ohmic resistance of the at least one electrical line with a threshold resistance value,

detect a breaking of the electrical line based on the comparison, and

~~such that~~ when a breaking of the electrical line is detected, ~~data is~~ automatically initiate the deletion of data ~~deleted~~ from at least one memory of the integrated circuit.

2. (Previously Presented) The integrated circuit according to claim 1, wherein the function modules comprise a random-number generator.

3. (Previously Presented) The integrated circuit according to claim 1, wherein the function modules comprise a first memory in which cryptological keys are stored.

4. (Previously Presented) The integrated circuit according to claim 3, wherein cryptological keys which are stored in the first memory are generated by means of the random-number generator.

5. (Previously Presented) The integrated circuit according to claim 1, wherein function modules comprise a real-time clock.

6. (Previously Presented) The integrated circuit according to claim 1, wherein operating parameters to be monitored additionally is the clock frequency of the real-time clock and/or an operating temperature at a point in the integrated circuit and/or an operating voltage of the integrated circuit.

7. **(Cancelled)**

8. (Previously Presented) The integrated circuit according to claim 1, wherein it is arranged in a package and has terminal contacts brought out of the package.

9. (Previously Presented) The integrated circuit according to claim 1, wherein individual function modules have an essentially planar extent and are arranged adjacently to one another in the area of the normal to the surface.

10. (Previously Presented) The integrated circuit according to claim 1, wherein the function modules comprise an integrated voltage regulator which regulates an operating voltage.

11. (Previously Presented) The integrated circuit according to claim 1, wherein it is constructed as semiconductor chip.

12. (Previously Presented) The integrated circuit according to claim 11, wherein semiconductor structures of the individual function modules are intermeshed in the manner of a puzzle in order to avoid individual function modules from being recognizable.

13. **(Currently Amended)** The integrated circuit according to claim 11, wherein an active protective layer which consists of at least one elongated electrical line which extends along the surface of ~~the die~~ a die of the semiconductor chip, particularly in mutually parallel tracks section by section, is applied directly to the die of the semiconductor chip.

14. (Previously Presented) An arrangement comprising an integrated circuit as claimed claim 1, wherein the integrated circuit is connected by means of a data bus to a second memory in which data are stored encrypted, wherein the second memory has memory cells which in each case have a memory address and each memory cell can be addressed directly in reading or writing manner.

15. (Previously Presented) The arrangement comprising an integrated circuit as claimed claim 14, wherein the second memory is volatile and is connected to a battery so that the voltage supply is maintained when another power supply is lacking.

16. (Previously Presented) The arrangement comprising an integrated circuit as claimed claim 1, wherein the integrated circuit is connected by means of a data bus to a non-volatile third memory in which data or program code are stored encrypted.

17. (Previously Presented) The arrangement comprising an integrated circuit according to claim 1, wherein the security sensor system is connected to a battery so that the voltage supply is maintained if another power supply is lacking.

18. (Previously Presented) The arrangement comprising an integrated circuit according to claim 1, wherein the security sensor system is connected to an auxiliary power source, integrated in the package, which provides the power for deleting the first memory.

19. (Previously Presented) The arrangement comprising an integrated circuit as claimed claim 16, wherein the third memory is a Flash memory or ROM.

20. **(Currently Amended)** An integrated circuit comprising function modules, wherein the function modules comprise:

a central processing unit designed to process data and to execute programs, **and**

a cache memory, ~~wherein the function modules comprise~~

an encryption unit designed to encrypt and decrypt data and the function modules comprise a security sensor system including a protective layer on the integrated circuit including at least one elongated electrical line extending along the surface of the integrated circuit, the security sensor system operable to monitor the state of a the protective layer on the integrated circuit such that when a breaking of the electrical line is detected, data is automatically deleted from at least one memory of the integrated circuit, ~~wherein the function modules comprise~~

a random-number generator and a first memory in which cryptological keys are stored, and wherein cryptological keys which are stored in the first memory are generated by means of the random-number generator, **and**

an integrated voltage regulator that regulates an operating voltage or current of the integrated circuit to render the operating voltage or current noisy to an outside observer, thus preventing attacks based on examination of the current of the integrated circuit.

21. **(New)** An integrated circuit system including:
an integrated circuit comprising:
a central processing unit designed to process data and to execute programs,
a first memory storing a cryptographic key,
an encryption unit designed to encrypt and decrypt data using the cryptographic key stored in the first memory,
a security sensor system including a protective layer covering the integrated circuit and a monitoring system that monitors the state of the protective layer covering the integrated circuit such that when a particular state of the protective layer is detected, data is automatically deleted from at least one memory of the integrated circuit, and
at least one terminal contact extending through the protective layer covering the integrated circuit, and
an external second memory outside the protective layer covering the integrated circuit and connected to the integrated circuit via the at least one terminal contact extending through the protective layer, and connected to the encryption unit of the integrated circuit via a data bus extending through the at least one terminal contact, the external second memory storing data encrypted with the cryptographic key stored in the first memory,
wherein the encryption unit is designed to read data or code out of the external second memory, decrypt the data or code using the cryptographic key stored in the first memory, and write the decrypted data or code into the first memory or other memory of the integrated circuit.